Getting Started With SHARC® Processors

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PREFACE

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The primary audiences for this guide are system designers, programmers, and hardware engineers who want to learn whether a specific SHARC processor matches design requirements for new applications.

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Manual Contents

This manual consists of:

- Chapter 1, "Introduction to SHARC Processors"

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- Visit the Embedded Processing and DSP products Web site at http://www.analog.com/processors/technical_support
- E-mail tools questions to processor.tools.support@analog.com

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- E-mail processor questions to
  processor.support@analog.com (World wide support)
  processor.europe@analog.com (Europe support)
  processor.china@analog.com (China support)

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ADSP-21465 ADSP-21467 ADSP-21469

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The list of supported SHARC processors is subject to change. For a complete and up-to-date listing of SHARC processors refer to:

http://www.analog.com/sharc

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code examples, and more.

Visit MyAnalog.com to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

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VisualDSP++ Online Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, Dinkum Abridged C++ library, and FLEXnet License Tools software documenta-

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sors/technical_library, navigate to the manuals page for your processor, click the request CD check mark, and fill out the order form.

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Data sheets, which can be downloaded from the Analog Devices Web site, change rapidly, and therefore are not included on the technical library CD. Technical manuals change periodically. Check the Web site for the latest manual revisions and associated documentation errata.

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1 INTRODUCTION TO SHARC PROCESSORS

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offering fixed- and floating-point computational power to 450 MHz/2700 MFLOPs. Regardless of the specific product choice, all SHARC processors provide a common set of features and functionality usable across many signal processing markets and applications. This baseline functionality

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enables the SHARC user to leverage legacy code and design experience, while transitioning to higher-performance, more highly integrated SHARC products.

By integrating on-chip, single-instruction, multiple-data (SIMD) process-

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on-chip peripherals such as sample rate conversion, S/PDIF transmitter/receiver, and BGA and LQFP package options.

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- **Automotive audio applications.** The ADSP-21362, ADSP-21365, ADSP-21369, ADSP-21371, ADSP-21462, ADSP-21465, and ADSP-21469 processors, with integration of sample-rate conversion, DTCP cipher, precision clock generators, and serial ports, are

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plify product development and reduce time to market.

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Common Architectural Features

SHARC processors share the following architectural features.

- 32/40-bit IEEE floating-point math

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  IEEE floating-point computation units–multiplier, arithmetic logic unit (ALU), shifter, and data register file

- Program sequencer with related instruction cache, interval timer, and data address generators (DAG1 and DAG2)

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- An SDRAM controller that provides an interface to as many as four separate banks of industry-standard SDRAM devices
- Up to a maximum of 5M bits of on-chip SRAM and up to 4M bits of on-chip, mask-programmable ROM

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transfers, remains. All four generations of SHARC processors are still in production, offering a variety of code-compatible options to meet a wide array of price, performance, and footprint requirements.

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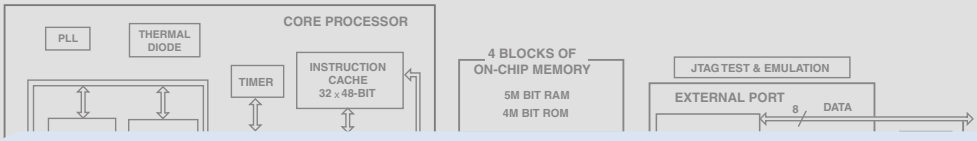

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data register files, significantly increasing overall system performance in a variety of applications. This capability is especially relevant in consumer, automotive, and professional audio where the algorithms related to stereo channel processing can effectively utilize the SIMD architecture.

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Third generation SHARC products employ an enhanced SIMD architecture that extends CPU performance to an impressive 400 MHz/2.4 GFLOPS. These products also integrate a variety of ROM configurations and audio-centric peripherals designed to decrease time to market and

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Integration of peripherals continue with serial ports, SPI ports, S/PDIF Tx/Rx, and an 8-channel asynchronous sample rate converter block. The fourth generation SHARC allows data from the serial ports to be directly transferred to external memory by the DMA controller again preserving internal memory space for code and data. The fourth generation processor

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also incorporates link ports that allow processor to processor communication for data movement. In addition, a number of fourth generation processors are also pin compatible for use with a single hardware platform.

Each SHARC processor provides unique capabilities, while being

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This balance of core speed, memory integration, and I/O bandwidth achieves the sustained performance critical to real-time applications.

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Table 1-1. ADSP-2126x SHARC Processor Specifications

	ADSP-21261	ADSP-21262	ADSP-21266
Frequency (MHz)	150	200	200

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Table 1-2. ADSP-2136x/ADSP-2137x SHARC Processor Specifications

	ADSP-21362	ADSP-21363	ADSP-21364	ADSP-21365	ADSP-21366	ADSP-21367	ADSP-21368	ADSP-21369	ADSP-21371	ADSP-21375
Frequency (MHz)	333	333	333	333	333	266,	333,	266,	266	266
										M bit
										M bit
										C to 0°C

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Table 1-3. ADSP-2146x SHARC Processor Specifications

	ADSP-21462	ADSP-21465	ADSP-21467	ADSP-21469
Frequency (MHz)	400	400	450	450
IIR Accelerators	Yes	Yes	Yes	Yes
FFT Accelerators	Yes	Yes	Yes	Yes
Link Ports	2	2	2	2
Thermal Diode	Yes	Yes	Yes	Yes

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Table 1-3. ADSP-2146x SHARC Processor Specifications (Cont'd)

	ADSP-21462	ADSP-21465	ADSP-21467	ADSP-21469
DDR2 Interface	Yes	Yes	Yes	Yes

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2 THE EVALUATION PROCESS

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on a SHARC processor. Development boards typically provide expansion headers, allowing you to prototype basic hardware without customized user hardware.

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"Selecting Software Development Tools" provides a summary of the available software development tools for SHARC processors. Most development tools available for SHARC processors provide a cycle accurate simulator which can develop initial algorithms and applications

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management of projects from start to finish from within a single interface.

Because project development and debugging is integrated, you can move quickly and easily between editing, building, and debugging activities. Key features include the native C/C++ compiler, advanced graphical plotting tools, statistical profiling, and the VisualDSP++ Kernel (VDK),

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Decide to evaluate SHARC
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http://www.BDTIC.com/ADI
- Purchase JTAG emulator pod.

Figure 2-1. Tool Selection Workflow

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which allows a user's code to be implemented in a more structured and easier to scale manner. Other features include assembler, linker, libraries, loader, splitter, cycle-accurate and functional-accurate compiled simulators, emulator support, and more. VisualDSP++ offers programmers a

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compiler supports a broad range of pragmas that allow the programmer to better exploit the compiler while maintaining C language neutrality. Just as important, the compiler has the ability to feed back advisory information to the programmer, offering further improvements to a code sequence, should the programmer be able to make certain guarantees

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about it. This information is displayed seamlessly in the VisualDSP++ main editor window. This removes the black box label that compilers sometimes have.

Backing the compiler is a powerful assembler and linker technology. Pro-

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The VisualDSP++ kernel (VDK) is a robust, royalty-free, real-time operating system (RTOS) kernel. This pre-emptive multitasking kernel incorporates state-of-the-art scheduling and resource allocation techniques tailored specifically for the memory and timing constraints of DSP programming. The kernel facilitates development of performance-structured

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applications using frameworks of template files. It provides essential kernel features in a minimal footprint. Features include a fully pre-emptive scheduler (time slicing and cooperative scheduling are also supported), thread creation, semaphores, interrupt management, inter-thread messag-

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VisualDSP++ excels in this regard, with best-in-class debugging and inspection support. Robust fundamental C language source debugging (source-level stepping and breakpoints, stack unwinds, local variable and C expression support, memory and register windows) serves as a foundation upon which multiple innovative and unique tools rest.

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VisualDSP++ supports a variety of debugging targets. Most common is a JTAG connection to an EZ-KIT Lite board or to a custom target board by means of Analog Devices emulator products. However, there will be occasions where closer inspection in a simulated environment may be required.

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windows can be made to “float” their focus to whichever processor currently is the debugger’s focus, or they can be “pinned” to a specific processor so their contents do not follow the debugger’s focus. To further aid MP debug, synchronous run, step, halt, and reset are also provided.

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The patented statistical profiler from Analog Devices offers unprecedented and unique visibility into a running application. Operating completely non-intrusively to the application, the application is polled thousands of times per second and a statistical view of where an application is spending

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able to connect to any SCC provider that supports the Microsoft® common source code control (MCSCC) interface. This interface is supported by all leading SCC vendors. VisualDSP++ goes one step further by supporting the control of VisualDSP++ itself within a source code control system.

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The ability to robustly test an embedded application is enabled through a comprehensive automation application programming interface (API). Using Microsoft's language-neutral automation technology, nearly every feature of the graphical environment is available to script authors. Appli-

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remains free regardless of how long you have owned your software.

Major and minor upgrades and updates to VisualDSP++ are also free and are released through the Analog Devices Web site.

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The Collaborative

The VisualDSP++ environment enables independent third-party companies to add value using the published set of application programming interfaces (APIs) from Analog Devices. The Collaborative™ is an inde-

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Table 2-1 provides information about SHARC processor evaluation kits. For additional information, visit the following Analog Web site:

http://www.analog.com/processors/sharc

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Table 2-1. SHARC Processor Evaluation Kits

Processor	Evaluation Kit/Reference Board	Daughter Board
ADSP-21261 ADSP-21262	21262 EZ-KIT Lite Desktop Evaluation Board	- EZ-Extender Daughter Board - USB EZ-Extender Daughter Board

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Software Modules

Analog Devices has a wide range of tested and optimized software modules available, including decoders, encoders, codecs and other algorithms that provide multimedia functions for the Blackfin family. The software modules allow engineers to quickly and easily incorporate these functions,

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providing a faster development path to the end product. In addition, the highly-optimized software modules feature a consistent API and framework to ensure rapid development of multiple functions.

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tered, yields full VisualDSP++ license status for 90 days from the date of installation. After 90 days, the license changes to restricted status, which limits the size of the application that can be built and supports debug

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agent connectivity only. Refer to "Software Development on SHARC Processors" on page 2-39 to see where the EZ-KIT Lite fits into the phases of program development.

Most EZ-KIT Lite boards include three expansion connectors configured

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ADSP-21262 EZ-KIT Lite From Analog Devices

Part Number: ADZS-21262-EZLITE

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wide range of applications.

The ADSP-21262 EZ-KIT Lite evaluation system includes an ADSP-21262 SHARC processor desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a

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USB-based PC-hosted tool set. With this EZ-KIT Lite, you can learn more about Analog Devices ADSP-21262 SHARC processor hardware and software development and prototype applications. The EZ-KIT Lite provides an evaluation suite of the VisualDSP++ integrated development

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- Evaluation suite of VisualDSP++ development tools
- 0-ohm resistor for current measurement
- Flash programmer utility for downloading boot code to on-board flash memory

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- Type A expansion interface with three connectors supporting parallel port, FLAG, SPI, and DAI interfaces
- 12 LEDs: 1 power (green), 1 board reset (red), S/PDIF (amber), 1 USB monitor (amber), and 8 general-purpose (amber)

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ADSP-21364 EZ-KIT Lite From Analog Devices

Part Number: ADZS-21364-EZLITE

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evaluation of ADSP-21364/5/6 SHARC processors.

The EZ-KIT Lite includes an ADSP-21364 SHARC processor desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a USB-based PC-hosted tool set. With this EZ-KIT Lite, users can learn more about ADSP-21363/21364/21365/21366

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SHARC processor hardware and software development and prototype applications. The ADSP-21364 EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C/C++ compiler, assembler, loader, and linker. All software tools are limited to use with the EZ-KIT Lite.

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flash memory

- Type A expansion interface with three connectors supporting parallel port, FLAG, SPI, and DAI interfaces

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- 4 programmable flags
- 11 LEDs: 1 power (green), 1 board reset (red), 1 USB monitor (amber), and 8 general-purpose (amber)

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ADSP-21369 EZ-KIT Lite From Analog Devices

Part Number: ADZS-21369-EZLITE

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The ADSP-21369 EZ-KIT Lite, as shown in as shown in Figure 2-4, provides a cost-effective method for initial evaluation of the ADSP-21367/21368/21369 SHARC processors via a USB-based PC-hosted tool set.

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- 1 x 2 RCA jack for 1 channel of stereo audio input
- Headphone jack (connected to one of the stereo outputs)
- SPDIF In RCA jack

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- SPDIF Out RCA jack
- ADM3202 RS-232 driver/receiver
- USB interface

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- CE certified

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ADSP-21375 EZ-KIT Lite From Analog Devices

Part Number: ADZS-21375-EZLITE

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The ADSP-21375 EZ-KIT Lite evaluation system, as shown in Figure 2-5, provides developers with a cost-effective method for initial evaluation of the ADSP-21371/21375 SHARC processors.

The ADSP-21371/21375 SHARC processors, which are pin-com-

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ADM3202 RS-232 line driver/receiver

- Parallel port, SDRAM control, flags, DAI, DPI
- ELVIS interface
- Stereo in/stereo out RCA jack

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- USB interface
- JTAG ICE 14-pin header
- Evaluation suite of VisualDSP++ development tools

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ADSP-21469 EZ-KIT Lite From Analog Devices

The ADSP-21469 EZ-KIT Lite (photo not available at time of publication) provides a cost-effective method for initial evaluation of the ADSP-21462/21465/21467/21469 SHARC processors via a USB-based

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- 2 x 2 RCA jack for 2 channels of stereo audio input
- 2 DB25 connectors for differential inputs/outputs
- Headphone jack (connected to one of the stereo outputs)

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- SPDIF In RCA jack
- SPDIF Out RCA jack
- ADM1032 two-wire sensor

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EZ-KIT Lite Expansion Boards

EZ-KIT Lite expansion boards enhance and extend EZ-KIT Lite features and functions. This section describes the SHARC EZ-Extender daughter board and the SHARC USB daughter board.

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Figure 2-6. SHARC EZ-Extender

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The SHARC EZ-Extender daughter board, as shown in Figure 2-6, is a separately sold assembly that plugs into a SHARC EZ-KIT Lite evaluation system's expansion interface. The extender aids the design and prototyping phases of SHARC processor-targeted applications.

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- Dimensions: 5 in. x 5 in.

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SHARC USB EZ-Extender

Part Number: ADZS-SHRCUSB-EZEXT

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The SHARC USB EZ-Extender daughter board, as shown in Figure 2-7, provides a solution for users to evaluate different peripherals on SHARC processors.

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The SHARC USB EZ-Extender daughter board allows developers to connect to the parallel port on the ADSP-21262 and ADSP-21364 EZ-KIT Lite and to the asynchronous memory bus on the ADSP-21369 EZ-KIT Lite and the ADSP-21375 EZ-KIT Lite. The EZ-Extender has peripherals

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JTAG Emulators

JTAG (Joint Test Action Group) is defined by the IEEE 1149.1 standard for a test access port for testing electronic devices. This standard defines a method for serially scanning the I/O status of each pin on the device as

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High-Performance USB 2.0 JTAG Emulator

Part Number: ADZS-HPUSB-ICE

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ble, non-intrusive, target-based debugging solution for Analog Devices JTAG processors.

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These easy-to-use USB-based emulators perform a wide range of emulation functions, including single-step and full-speed execution with predefined breakpoints, and viewing and/or altering of register and memory contents. With the ability to automatically detect and support

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- Support for all ADI JTAG processors
- Multiple processor I/O voltage support with automatic detection
- 1.8 V, 2.5 V, and 3.3 V compliant and tolerant

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- 5 V tolerant and 3.3 V compliant for 5 V processors
- Multiprocessor support
- 14-pin JTAG connector

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USB 1.1 JTAG Emulator

Part Number: ADZS-USB-ICE

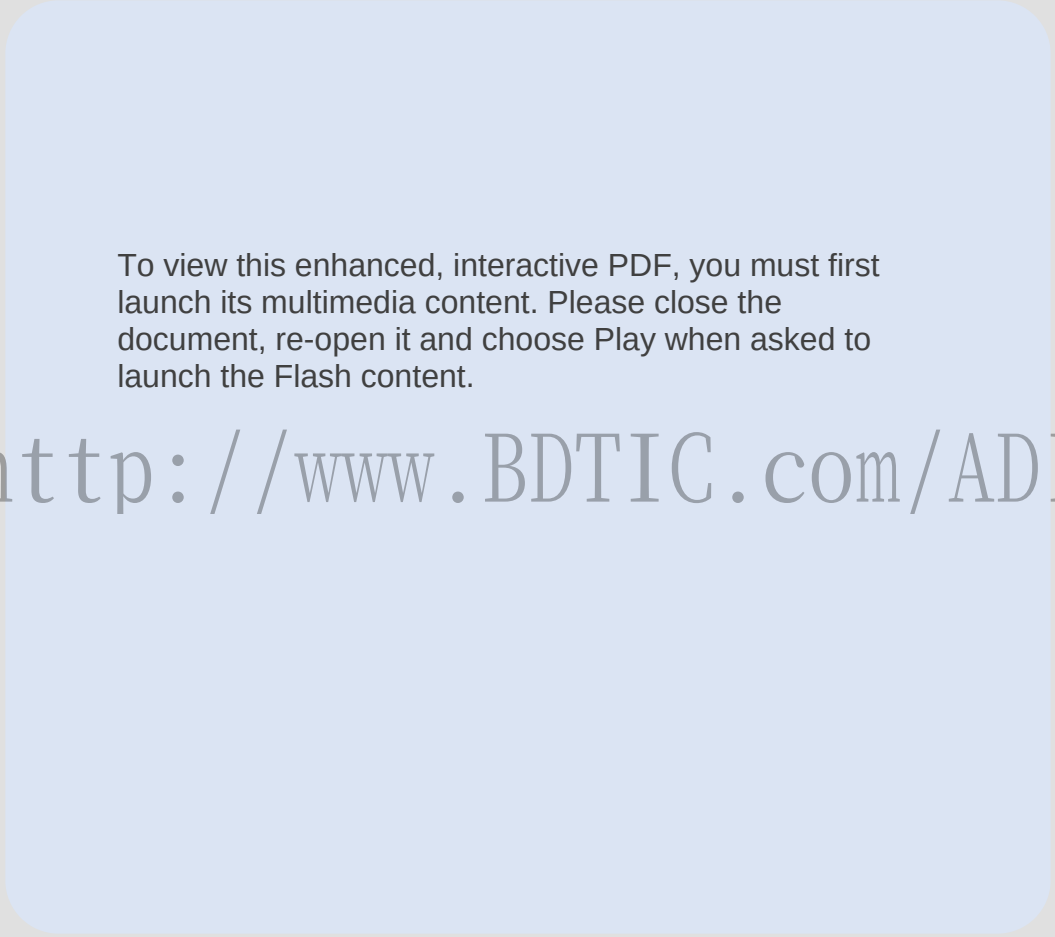
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Figure 2-9, from Analog Devices provides a portable, non-intrusive, target-based debugging solution for Analog Devices JTAG processors.

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This USB-based emulator performs a wide range of emulation functions, including single-step and full-speed execution with predefined breakpoints, and viewing and/or altering of register and memory contents. With the ability to automatically detect and support multiple I/O volt-

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- 5 V tolerant and 3.3 V compliant for 5 V processors
- Multiprocessor support

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- 14-pin JTAG connector
- 3-meter USB cable for difficult to reach targets

Selecting the Right Combination of Tools

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http://analog.com/processors/tools/testdrive

When the TestDrive license expires, consider purchasing a full seat of VisualDSP++ (p/n: VDSP-SHARC-PC-FULL).

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After you have finished constructing your hardware, purchase a low-cost USB emulator (p/n: ADZS-USB-ICE) from Analog Devices.

Scenario 2

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a JTAG emulator. Emulators enable you to perform the debug operations that you may have performed previously on a development board on your own custom hardware.

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3 SUPPORT OPTIONS

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available.

- Processor and development tools selection guides
- Additional getting started information
- Applications notes, EE-notes, and other articles

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- Communities-related information
- Platform-related information

Visit the SHARC processor home page at: http://www.analog.com/sharc.

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data available from independent testers. A link to training and events provides an up-to-date list of local training seminars and upcoming events where you can learn more about all SHARC processor products.

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Applications Notes, EE-Notes, and Other Articles

The most useful documents available to users are the Application or EE-(Engineer-to-Engineer) Notes, since they offer detailed technical information about using the SHARC processor. These materials may be

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Workshops and Seminars

The most efficient way to learn about the SHARC processor architecture is by attending a 3½-day (or 1-day) SHARC seminar. These seminars provide a mixture of lectures and demonstrations. The 3½-day workshop

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pricing information at:

http://www.kaztek.com

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SHARC Processor Seminars

The SHARC processor seminar is a subset of the SHARC Processor Workshop slide set and does not include hands-on exercises. A SHARC seminar is often accompanied by tools and software demonstrations run-

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erence manual and provides powerful search facilities to help you locate information.

You can find SHARC processor hardware reference manuals at:

http://www.analog.com/processors/manuals

www.BDTIC.com/ADI

Programming Reference

The programming reference contains information about the processor architecture and assembly language for SHARC processors. The manual provides information on how assembly instructions execute on the

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To obtain data sheets for SHARC processors, open your browser and access:

http://www.analog.com/sharc

www.BDTIC.com/ADI

Anomalies Lists for Processors and Tools

Analog Devices maintains an anomalies list for each subfamily of SHARC processors and also maintains an anomalies list for tools. These documents are updated as new information becomes available.

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IBIS-based simulators for transmission line simulation of digital systems. These models accurately simulate I/O buffers, termination, and circuit board traces. The simulation time is much faster than SPICE simulations,

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because it is a behavioral model that relies on tabulated current versus voltage characteristics. For more information about IBIS models, see the main ANSI/EIA IBIS home page at:

http://www.eigroup.org/IBIS

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VisualDSP++ Help incorporates a searchable version of the VisualDSP++ manual set plus processor documentation and other tools manuals. See "VisualDSP++ Help" on page 3-13 for details.

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VisualDSP++ Getting Started Guide

This manual provides step-by-step, 15-minute tutorials that highlight VisualDSP++ features. By completing the tutorials, users can become familiar with the VisualDSP++ environment quickly, and see how easy it

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This manual contains information about the C/C++ compiler and its features designed for use with SHARC processors. It includes syntax for command lines, switches, and language extensions. It leads you through the process of using library routines and writing mixed C/C++/assembly code.

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VisualDSP++ Runtime Library Manual for SHARC Processors

This manual contains information about the C/C++ and DSP run-time libraries for SHARC processors. It leads you through the process of using library routines and provides information about the ANSI standard header

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real-time operating system kernel integrated with the VisualDSP++ development tools. The VDK incorporates state-of-the-art scheduling and resource allocation techniques tailored specifically for the memory and timing constraints of DSP programming. Using frameworks of template

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files, the kernel facilitates development of performance-structured applications. The kernel is designed for effective operations on Analog Devices processors.

The majority of the information in this manual is generic to all Analog

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[<install_path>]:\Program Files\Analog Devices\VisualDSP 5.0\211xx\Examples

[<install_path>]:\Program Files\Analog Devices\VisualDSP 5.0\212xx\Examples

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```
[<install_path>]:\Program Files\Analog Devices\VisualDSP
5.0\213xx\Examples
```

Hardware Tools Documentation

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the software on your PC. This manual also provides guidelines for running your own code on the SHARC EZ-KIT Lite. In addition, the manual describes the operation and configuration of the evaluation board's

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components. Finally, a full design database (schematics, layout, and a bill of materials) is provided as a reference for future SHARC processor board designs.

This manual provides information on the EZ-KIT Lite from a program-

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VisualDSP++ Help, built around the familiar Microsoft HTML Help standard, enables you to:

- Copy code examples from Help into your source documents

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- E-mail processor questions to
  processor.support@analog.com (World wide support)
  processor.europe@analog.com (Europe support)
  processor.china@analog.com (China support)

www.BDTIC.com/ADI

- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, local sales office or authorized distributor

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